AMEYA CENTRE FOR ROBOTICS & EMBEDDED TECHNOLOGY

(acret)

MUMBAI

Detailed Syllabus for VHDL Programming on Xilinx Spartan 3 FPGA

1. Review of Programmable devices such as ROM, PAL, PLD etc.
2. Introduction to CPLD and FPGA, Comparison between the two.
3. Introduction to Xilinx CPLD
4. Introduction to Xilinx Spartan 3 FPGA
5. Introduction to VHDL:
   The origins of VHDL, VHDL basics, Benefits of VHDL, VHDL levels of abstraction, Abstraction and timing, VHDL in the system design flow, The VHDL design flow, VHDL synthesis, Modeling hardware in VHDL, VHDL design entities, Entity declarations, Architectures, Using libraries and packages, Concurrent signal assignments, Signal assignments with delays
6. Hierarchy in VHDL:
   Component declarations, Component instantiation, Named port mapping, Positional port mapping, Direct instantiation, Configuration specifications, Entity binding, Port modes
7. VHDL processes, Processes sensitivity lists, Test benches
8. Objects and Data Types:

Objects in VHDL, Constants, variables and signals, VHDL types, Scalar types, Arrays, Records, Synthesis of ints and enums, Custom types and subtypes, Tristate and resolved types, std_ulogic and std_logic, unsigned and signed, Attributes.

9. Concurrent and Sequential Statements:

Concurrent statements, Sequential statements, Conditional & selective signal assignments, The generate statement, Signal and variable assignments, Synthesis of statements, Latch inference, For loops & loop synthesis

10. Simulation and Synthesis:

How a VHDL simulator works, Event driven simulation, Event processing, Simulation (delta) cycles, Delta cycle race conditions, Elaboration, Process synthesis, Synthesizable processes styles & templates, Combinational logic in a process, Synchronous (clocked) processes

11. Finite State Machines (FSMs):

Review of Moore and Mealy state machines, Finite state machines representation, Use of enums to represent state, FSM code structure, FSM, example of FSM

12. FSM implementation example, Synthesis of FSMs

13. Subprograms and Packages:

Subprograms, Functions, Procedures, Differences between functions and procedures, Subprogram declarations, Packages, Package declaration, Package body, Example: color package

14. Configurable and Scalable Designs:

Generic parameters, Generic mapping, Example: generic word length, Configuration declarations, Default binding, Example Configuration Declaration, Assertions,

Laboratory Work

1. Introduction to Mentor Graphics ModelSim for VHDL, simulation, Introduction to Xilinx ISE for synthesis & implementation,

2. Introduction to programmable devices boards (FPGA, CPLD) along with the main board features and the use of programming tools (Xilinx ISE & ModelSim).
3. Implementation of basic logic gates and its testing.
4. Implementation of adder circuits and its testing.
5. Implementation 4 to 1 multiplexer and its testing.
6. Implementation of 3 to 8 decoder and its testing.
7. Implementation of J-K and D Flip Flops and its testing.
8. Implementation of sequential adder and its testing.
9. Implementation of BCD counter and its testing
10. Implementation of two 8-bit multiplier circuit and its testing.
11. Generating regular repetitive structures
12. Finite impulse response filter
13. Finite state machine
14. Post synthesis + post place and route simulation
15. RAM board model
16. Direct Digital Synthesis (DDS)

At the end of the course, the last session will be devoted to recent developments in the field of VLSI Design, in industries across India and will include information on career opportunities in the field.